High Efficiency, Synchronous Dual-Ouputs Buck Converter

1 Description

The SC8102A is a synchronous dual-output ports buck converter with a wide input voltage from 5V to 36V. The SC8102A regulates the output voltage at a fixed 5V or customized voltage by setting the divider resistor. It also provides high accurate output current limit. The converter enters Constant Current (CC) Mode in case any of the two output channels reaches the setting current limit. The total output power can be programmed by a resistor, which makes it easy for constant power control.

The SC8102A adopts fixed line drop compensation, programmable frequency setting and PWM/PFM mode operation. It also integrates automatic DCP mode and Type-C current mode, so that a USB controller can be saved. With minimum external components, maximum functions can be achieved for user's different applications.

The SC8102A also supports full protections including under voltage protection, over voltage protection, short current protection and auto-restart, over temperature protection.

The SC8102A adopts 32 pin QFN 5x5 package.

2 Features

- Wide input operating voltage from 5V to 36V
- Max output capacity with 5V/6A
- 100% duty cycle operation
- Less than 200uA low quiescent current
- ±5% output current limit accuracy
- Programmable output power limit
- Build-in DP/DM for USB DCP modes:
  - BC1.2 DCP Mode
  - Divider Mode
  - 1.2V/1.2V Mode
- Build-in USB Type-C 3A current mode
- Integrated NMOS gate driver
- Build-in line drop compensation
- Adjustable frequency 80kHz to 600kHz
- Hiccup and auto-restart
- Full protection of UVLO, OVP, OCP, OTP
- Available in QFN-32 5x5 Package

3 Applications

- Car Charger
- Multi-Ports Wall Charger
- Hub
- Industrial applications

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8102AQDER	32 pin QFN	5 mm x 5 mm x 0.75 mm

5 Typical Application Circuit

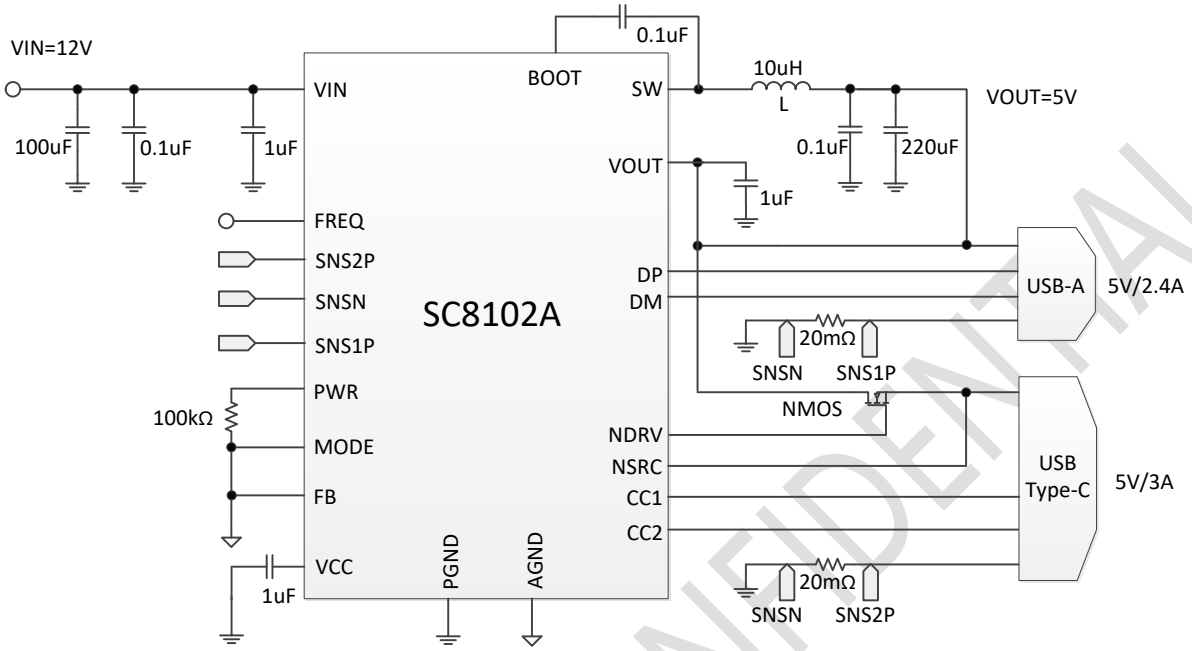


Figure. 1 Typical Application Circuit with Dual-Outputs and Isolated NMOS

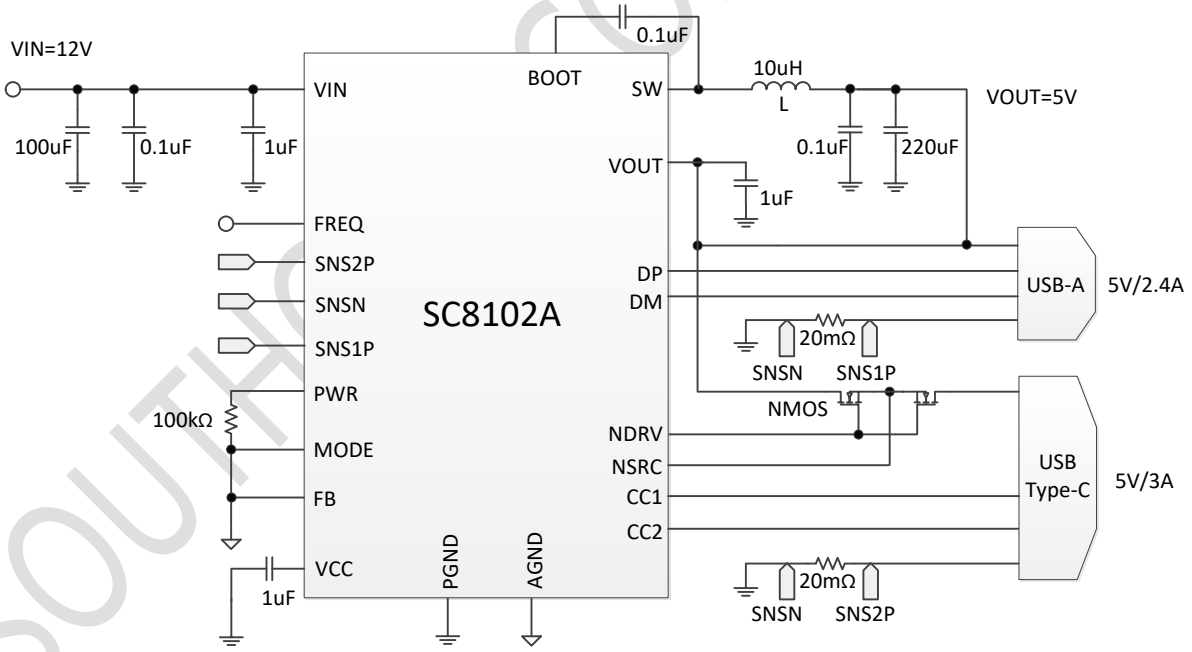
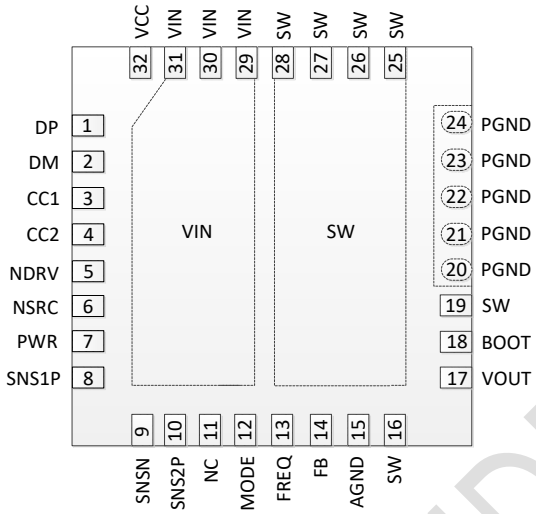


Figure. 2 Typical Application Circuit with Dual-Outputs and Back-to-Back Isolated NMOS

6 Terminal Configuration and Functions



QFN 32 Package Reference

(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	DP	I/O	D+ data line to USB connector 2, used for hand-shaking with portable devices.
2	DM	I/O	D- data line to USB connector 2, used for hand-shaking with portable devices.
3	CC1	I/O	Configuration Channel 1 to USB Type-C connector.
4	CC2	I/O	Configuration Channel 2 to USB Type-C connector.
5	NDRV	O	Gate signal for isolated Type-C NMOS
6	NSRC	O	Source signal for isolated Type-C NMOS
7	PWR	I	Output power limit pin. Setting the output power limit by connecting a resistor to GND with the following equation $P_{LIM\_OUT} = \frac{VREF}{R_{LIM}} \times 2 \times 10^6$
8	SNS1P	I	Positive end of output 1 current sense amplifier. The output current limit can be set as $I_{LIM\_OUT} = \frac{54mV}{RSNS}$
9	SNSN	I	Negative end of output current sense amplifier.
10	SNS2P	I	Positive end of output 2 current sense amplifier. The output current limit can be set as $I_{LIM\_OUT} = \frac{54mV}{RSNS}$
11	NC		Floating.

12	MODE	I	Mode selection pin. Logic high level sets the device working in PWM mode; logic low level or floating sets the device working in PFM mode.
13	FREQ	I	The operation frequency is programmed by a resistor between this pin and AGND. $$f_S(\text{kHz}) = \frac{20000}{R_{FREQ}(\text{k}\Omega)}$$ Leaving this pin floating sets the device working in 150kHz.
14	FB	I	Output voltage feedback. Connect the center of two divider resistor to program the output voltage. $$\text{VOUT} = \text{V}_{FB\_REF} \times \left(1 + \frac{\text{R}_{UP}}{\text{R}_{DOWN}}\right)$$ Output voltage be configured for fixed 5.05V with FB pin connected to GND.
15	AGND	I/O	Analog Ground.
17	VOUT	I	Output node of the Buck. Connect a 1 μF ceramic capacitor from VOUT to PGND pin.
18	BOOT	PWR	Connect a capacitor between BT and SW to bootstrap a voltage to provide the bias for high side MOSFET driver.
16, 19, 25, 26, 27, 28	SW	PWR	Switching node.
20~24	PGND	PWR	Power ground.
29, 30, 31	VIN	I	Input node of Buck. Connect a 1 μF ceramic capacitor from VIN to PGND pin.
32	VCC	PWR	Output of internal regulator to provide 5.2V voltage for the bias voltage of internal gate drivers. Connect a 1 μF ceramic capacitor from VCC to PGND pin.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, VOUT, SNS1P, SNSN, SNS2P,	-0.3	42	V
	SW	-1	42	V
	NDRV	-1	10	V
	FB, DP, DM, CC1, CC2, VCC, FREQ, MODE, NSRC, PWR	-0.3	6.5	V
	BOOT	-0.3	50	V
Temperature Range	Operating Junction, T_J	-40	150	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2) for DP/DM pin	-8	8	kV
	Human body model (HBM) ESD stress voltage(2) for CC1/CC2 pin	-8	8	kV
	Human body model (HBM) ESD stress voltage for other pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

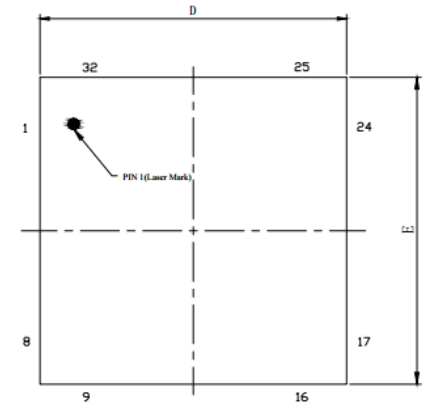
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

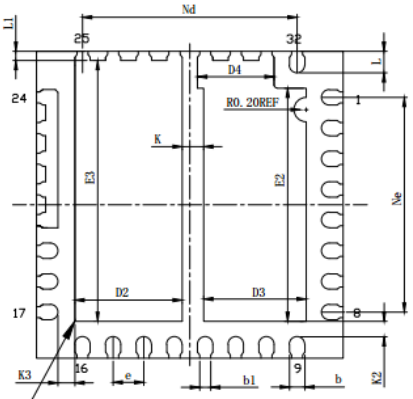
		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	5		36	V
V_{OUT}	Output voltage range	3		36	V
C_{IN}	Input Capacitance	30	100		μF
C_{OUT}	Output capacitance	30	220		μF
L	Inductance	2.2	10	22	μH
$R_{SNS1/2}$	Current Sensing Resistor	5	20	20	mΩ
f_{SW}	Operating frequency range	80	150	600	kHz
T_J	Operating junction temperature	-40		125	°C

Packaging Information

QFN32L(0505x0.75-0.50)

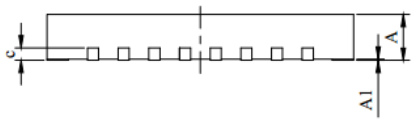


TOP VIEW



BOTTOM VIEW

EXPOSED THERMAL
PAD ZONE



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	4.90	5.00	5.10
D2	1.65	1.75	1.85
D3	1.575	1.675	1.775
D4	1.15	1.25	1.35
e		0.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
E3	4.15	4.25	4.35
Ne		3.50BSC	
L	0.30	0.35	0.40
K	0.30	0.35	0.40
K2	0.20	0.25	0.30
K3	0.225	0.275	0.325
R		0.02REF	