

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW[®]7726B is a synchronous rectifier controller, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. By driving an external MOSFET, JW7726B is able to significantly improve the efficiency comparing with the conventional Diode rectifier.

When JW7726B senses V_{ds} of MOSFET less than -300mV, it turns on the MOSFET. Once the V_{ds} is greater than -10mV, JW7726B turns off the MOSFET.

JW7726B supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW7726B is able to handle CCM operation.

JW7726B is available in SOT23-6 package..

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FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output voltage directly supply VCC
- Low quiescent current
- Fast driver capability for CCM operation
- SOT23-6 package

APPLICATIONS

- Active clamp Flyback and Flyback converters
- Adaptor
- LCD and PDP TV

TYPICAL APPLICATION

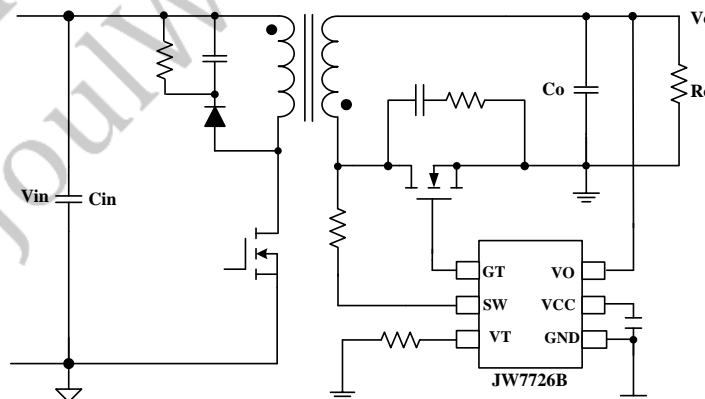


Figure A: JW7726B Typical Application for low-side.

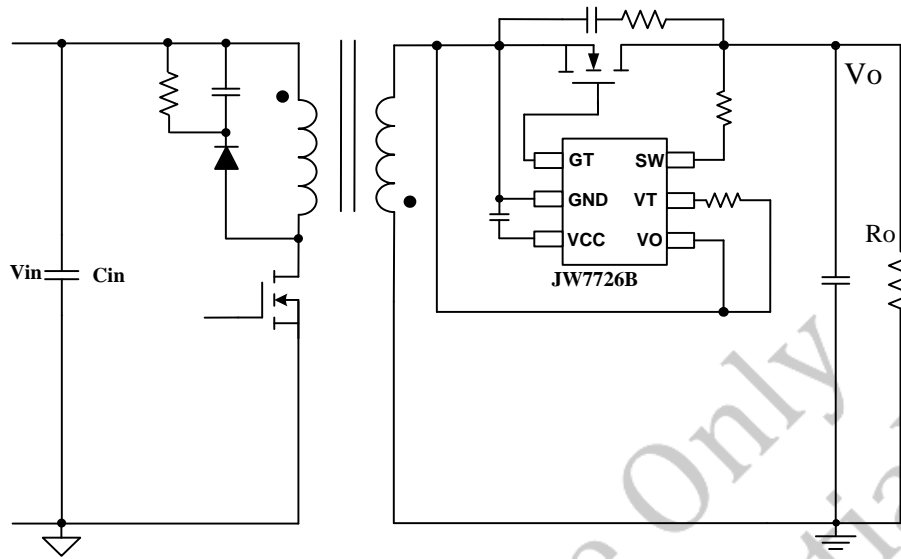


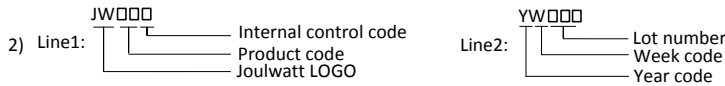
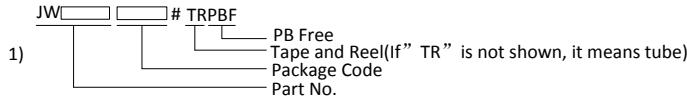
Figure B: JW7726B Typical Application for high-side.

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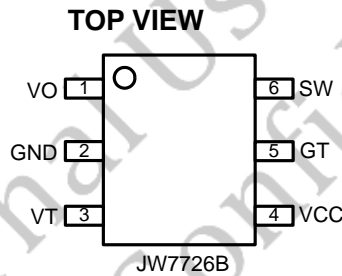
ORDER INFORMATION

TAPE AND REEL ¹⁾	PACKAGE	TOP MARKING ²⁾
JW7726BSOTB#TRPBF	SOT23-6	JWEW□ YW□□□

Notes:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

SW PIN	-1 to 130V
VO PIN	-0.3 to 30V
VCC, GT PIN.....	-0.3 to 10V
VT PIN.....	-0.3 to 7V
Continuous Power Dissipation($T_A=+25^{\circ}C$) ²⁾ SOT23-6.....	0.6W
Junction Temperature ³⁾	150°C
Lead Temperature	260°C
Storage Temperature.....	-65°C to 150°C
ESD Susceptibility (Human Body Model)	2kV

RECOMMENDED OPERATING CONDITIONS

SW Pin.....	4.7V to 120V
VO Pin.....	4.7V to 27V
VCC, GT PIN.....	4V to 8V
Operation Junction Temp.	-40°C to 125°C

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
SOT23-6.....	.220 ...130°C/W	

Note:

- 1) Exceeding these ratings may damage the device.
- 2) $T_A=25^\circ\text{C}$. The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(\text{MAX})$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(\text{MAX})=(T_J(\text{MAX})-T_A)/\theta_{JA}$.
- 3) The JW7726B guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 4) Measured on JESD51-7, 4-layer PCB.

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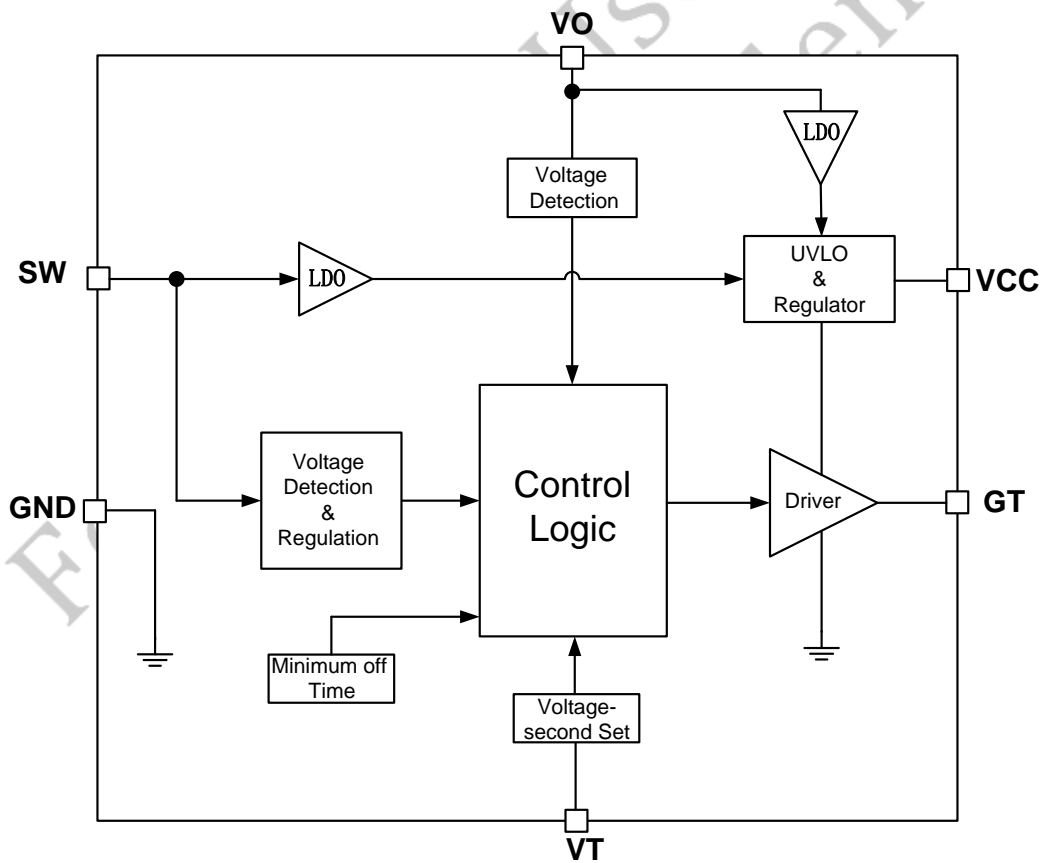
ELECTRICAL CHARACTERISTICS

<i>TA = 25°C, unless otherwise stated</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
<i>VCC Section</i>						
VCC Voltage	VCC	SW=40V, VCC=2.2uF	7.5	8	8.5	V
VCC Startup voltage	V _{CC_Startup}			4.5		V
VCC UVLO	V _{CC_UVLO}			3.9		V
Operation Current (Switching)	I _{SW}	GT=5nF, F _{sw} =100KHz		3.2		mA
Operation Current (GT On)	I _{VCC}	GT=5nF, VCC=2.2uF		900		uA
Quiescent Current	I _q	VCC=4.5V, VCC=2.2uF		70		uA
<i>Gate Section</i>						
Gate Turn on Threshold	V _{MOS_ON}			-150		mV
Gate Turn off Threshold	V _{MOS_OFF}			-10		mV
Gate Turn off Threshold in MOT	V _{GTOFF_MOT}			1		V
Gate Turn on Voltage	V _{GT}	SW=32V, VCC=2.2uF	V _{CC} -1	V _{CC}		V
Maximum Gate Pull up current	I _{GU}			0.65		A
Maximum Gate Pull down current	I _{GD}			4.7		A
Gate Minimum on Time	T _{MIN_ON}			500		ns
Absolutely Minimum off Time	T _{MIN_OFF}			350		nS
Turn off blanking threshold	V _{OFF_MIN_OFF}		2	2.5	3	V
Turn-on total delay	T _{DON}	R _{GATE} =0Ω, C _{LOAD} =4.7nF		50		nS
Turn-off total delay	T _{DOF}	R _{GATE} =0Ω, C _{LOAD} =4.7nF		20		nS
<i>SW and VO Section</i>						
VCC Charge Current	I _{SW_CHG}	SW=40V, VCC=6V		80		mA
SW Regulation Voltage	V _{MOS_REG}			-40		mV
SW Control Voltage MAX	V _{MOS_REG_MAX}			-160		mV
VO Enable Charge Voltage	V _{O_EN}	VCC=4V, SW=0V, rising		4.6		V
VO Disable Charge Voltage	V _{O_DIS}	VCC=4V, SW=0V, falling		4.5		V
VO Charge Current	I _{VO_CHG}	SW=0V, VCC=6V, VO=12V		40		mA

PIN DESCRIPTION

Part No.	Name	Description
5	GT	Drive the External NMOSFET.
2	GND	Ground.
4	VCC	Power supply. Bypass a Capacitor Between VCC and GND.
3	VT	Set the voltage-second product.
1	VO	Output Voltage Sensing and Charging to VCC.
6	SW	External Power MOSFET Drain Voltage Sensing. Charging to VCC.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7726B is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converters.

Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

When VO is lower than 4.5V (falling), JW7726B can power itself through the internal LDO connected to SW pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

When VO is above 4.6V (rising), the VO pin charges VCC pin.

Once the VCC voltage exceeds $V_{CC_Startup}$, the JW7726B exits the UVLO. If VCC is lower than V_{CC_UVLO} , the external MOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage $V_{cc_startup}$.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage $V_{cc_startup}$, the parts is activated again.

Turn On Phase

There are two conditions for the JW7726C to turn on the SR, i.e. V_{sw} , voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Fig. 1.

1) V_{sw} : when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW} across it. When V_{SW} is lower than V_{MOS_ON} , the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time T_{DON} if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Fig. 2.

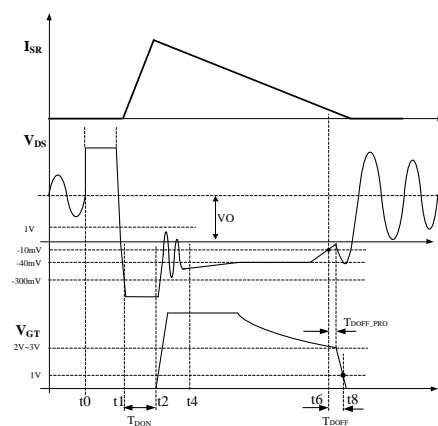


Figure. 1 Turn on delay and turn off delay

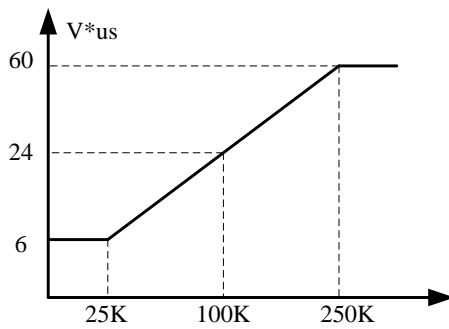


Figure-2 Volt-second value vs. VT resistance

Minimum On Time (MOT)

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The V_{SW} voltage may have a parasitic ring when the synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. Minimum on time is 500ns for high frequency applications. During the minimum time, the gate can still be turned off if V_{SW} touches a positive threshold value, +1V.

Conducting Phase

When the synchronous MOSFET is turned on, the drain source voltage V_{SW} it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the V_{sw} to a internal threshold (typical -40mV) after the synchronous MOSFET turn on. When the

V_{SW} is lower than -40mV, the gate keep its maximum voltage. And the synchronous MOSFET is fully on.

The V_{SW} rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the V_{SW} around -40mV.

It should be noted that the typical regulation threshold (-40mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

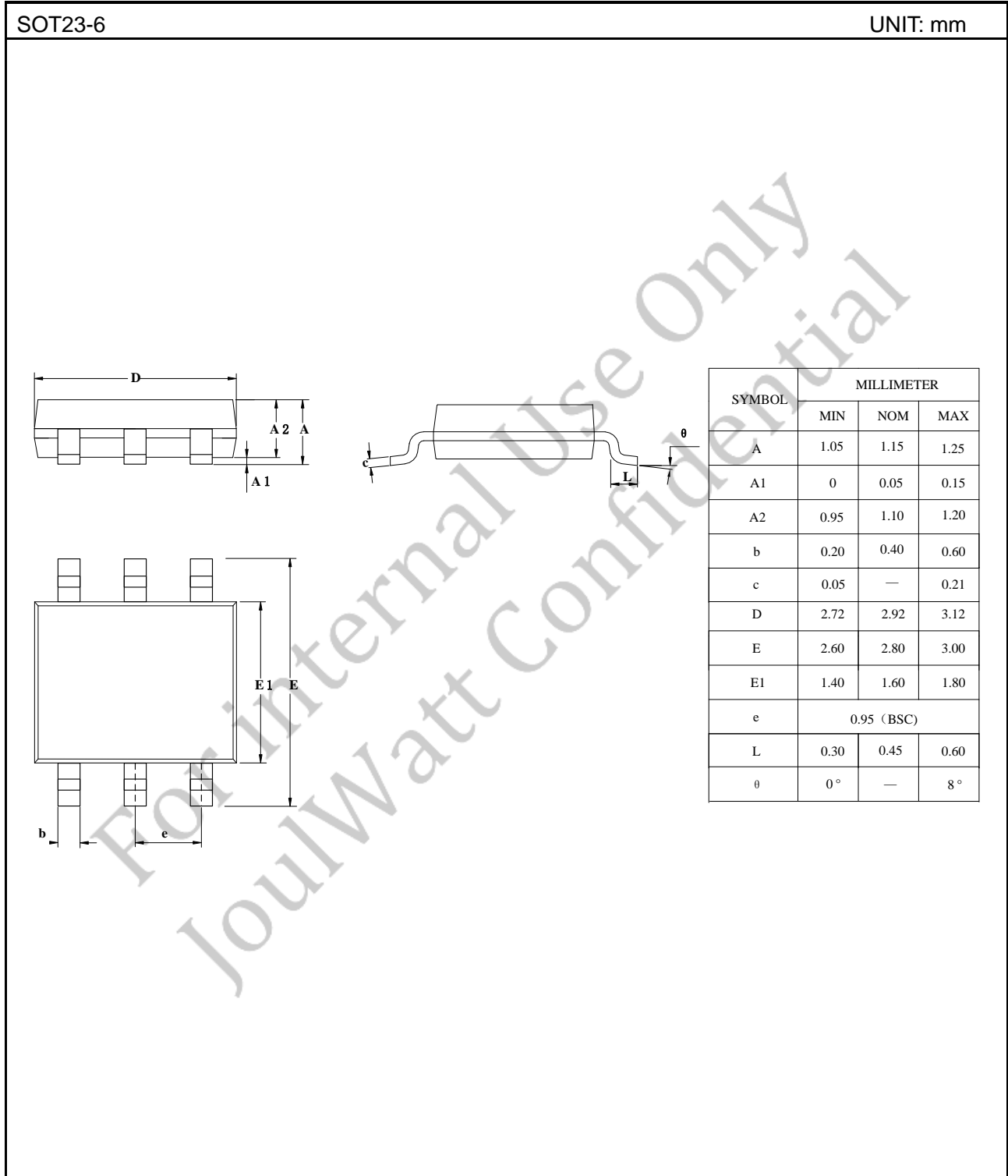
Turn Off Phase

After synchronous MOSFET conducting, once the voltage V_{SW} touches the MOSFET turn off threshold (-10mV), the gate is pulled to low after a turn off delay time T_{DOFF} . A 350nS blanking time is necessary to avoid error trigger. The banking time is reset once V_{sw} rises above 2V.

Output Voltage Detection

The JW7726B has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than 4.6V to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below 4.5V, the JW7726B is powered from SW pin.

PACKAGE OUTLINE



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